UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,593	09/26/2003	James R. Vogt	42P8647C	8662

			EXAMINER
8791	7590	12/22/2004	THAI, TUAN V

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/672,593	VOGT ET AL.
	Examiner	Art Unit
	Tuan V. Thai	2186

-- Th MAILING DATE of this communication appears on the cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _21 June 2004_.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _25-60_ is/are pending in the application.

    4a) Of the above claim(s) _1-24_ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _25-60_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _26 September 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
    application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)		4) ☐ Interview Summary (PTO-413)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)		Paper No(s)/Mail Date. _____ .
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)		5) ☐ Notice of Informal Patent Application (PTO-152)
Paper No(s)/Mail Date _6/21/2004_.		6) ☐ Other: _____ .

U.S. Patent and Trademark Office

PTOL-326 (Rev. 1-04)   Office Action Summary   Part of Paper No./Mail Date 12072004

Part III   DETAILED ACTION

Specification

1.   This office action responsive to communication filed June

21, 2004.   Claims 25-60 are presented for examination.   Claims 1-

24 have been canceled.

2.   Applicant is reminded of the duty to fully disclose

information under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs
of 35 U.S.C. ' 102 that form the basis for the rejections under
this section made in this Office action:

> A person shall be entitled to a patent unless -

> (b) the invention was patented or described in a printed
> publication in this or a foreign country or in public use or
> on sale in this country, more than one year prior to the
> date of application for patent in the United States.

4.   Claims 25-30, 32-43 and 45-48 are rejected under 35 U.S.C.

102(b) as being anticipated by Junya (USPN: 5,469,564);

As per claim 25, <u>Junya</u> teaches the invention as claimed

including a memory device 100 comprising a main memory array is

taught as flash memory array 10 (e.g. see figure 1; column 2,

lines 21 et seq.); an internal processor to execute programming

code is taught as the R/W control circuit 11 for executing

programming code from host computer 200 (e.g. see figure 1); a

hidden storage area connected to the main flash array wherein

the programming code prevents access to the hidden storage area

without a valid password is taught by Junya as the read/write

control circuit 11 functions to read passwords from the

data file area 16 of the memory 10 in response to address

signals generated by the address signal generator 13 based upon

the password addresses read from the password table area 15; the

comparing circuit 12 functions to compare the passwords read out

by the read/write control circuit 11 with the password supplied

by the host computer 200; wherein if the comparing circuit 12

detects a match, the data storage device 100 provides an access

permission signal to the host computer 200 for access to memory

10. (e.g. see abstract, column 2, lines 34 et seq.; lines 65

bridging column 3, line 4);

As per claims 26 and 27, Junya discloses main memory array

is a flash EEPROM; noting that Junya further discloses the type

of memory employed is NOT limiting to the present invention (e.g.

see column 2, lines 24-26);

As per claim 28; the further limitation of where the hidden

storage area of memory array 100 comprises one or more hidden

banks is taught by Junya to the extent that it is being claimed,

for example, as noted above, the type of memory is a system

depended feature, wherein as being illustrated by Junya; any

type of memory could be implemented including DRAM, RAM, FLASH,

which is known to comprise at least one segment/bank/portion as

being claimed (e.g. see column 2, lines 24-26);

As per claim 29; Junya discloses memory storage unit 10 having a password area 15 and a data file area 16 storing active (valid reference) passwords (e.g. see Junya's figure 1, column 2, lines 23-24);

As per claim 30, wherein the valid password allows accesses to only one of the users spaces (e.g. see Junya's column 2, lines 34 et seq.);

As per claim 32, Junya discloses the blocks/banks selector for selecting memory banks/blocks as being equivalent to the read/write control circuit 11 for decoding/selecting password data/addresses (e.g. see column 3, lines 24 et seq.);

As per claim 33, wherein the hidden storage area further comprises an output bus gate to prevent access to the hidden storage memory banks (e.g. see Junya's column 2, line 48 bridging column 3, line 4);

As per claims 34 and 35; wherein the hidden storage area comprises and address decoder for enabling the access (opening the bus gate) to the memory area when valid password and memory address are provided is taught by Junya as the comparing circuit 12 and read/write control circuit 11; and the valid memory address is provided by a host (e.g. see Junya's figure 1, column 2, lines 37 et seq.);

As per claim 36, the further limitation of the valid memory address is provided by the host is taught by Junya since starting at column 4, lines 30 et seq. discloses that starting (valid) memory address could be stored in a directory contained in the host computer 200;

As per claim 37, Junya discloses the password register bit is added to the password addresses to indicate whether the password is active for the purposes of verification (e.g. see column 3, lines 12 et seq.; also column 4, lines 3 et seq.);

As per claims 38 and 39, the further limitation of wherein the memory device connected to (or having) a bad password counter for counting the number of times the internal processor is unable to verity the password is taught by Junya as UP/DOWN counter which connected to the output of the comparator 41 for keeping track of number of the passwords being matched/NOT_matched (e.g. see column 3, lines 48-62);

As per claim 40, Junya discloses a method comprises storing one or more valid passwords in a hidden memory area is taught as active passwords are being stored in the data file area 16 (e.g. see column 3, lines 7-8); receiving a password at an internal processor connected to the hidden memory area is taught as password HC received from the host computer 200 connected to the data file area 16; and executing programming code to verify the

password against a valid reference password stored within the

hidden memory area is taught as the comparing circuit including

the digital comparator 41 for comparing passwords HC receiving

from the internal host 200 with a password MR read from the data

file area 16 of memory 10 (e.g. see column 3, lines 48-52);

As per claims 41 and 42, the further limitation of

permitting access to read/write from the hidden memory area if

the password is verified is equivalently taught by Juyna as

permitting external device access to the hidden data stored in

the data storage device if the passwords are compared and

verified (e.g. see column 4, lines 53-65);

As per claim 43; the further limitation of permitting

access to write to the hidden memory area if a valid address in

the hidden memory area is provided is taught by Juyna to the

extent that it is being claimed; for example, Juyna teaches that

password address must be decoded first to determine whether it

is active/valid address for proceeding to the comparison process

in determining as to whether the external device can access to

the hidden data stored in the data storage device (e.g. see

column 6, lines 48-58);

As per claims 45 and 48, Junya discloses that if the

password HC does not match the password MR (bad password), then

the output of the comparator 41 is drive low, the UP/DOWN counter

which also connected to the output of the comparator is in turn
will count in accordingly (depended on the user's setting) with
the outcome of the comparison results and set/reset the counter
accordingly (e.g. see column 3, lines 52-58); it should be noted
that when the correct/recovery is written, the UP/DOWN counter is
known to be reinstated/reset as being claimed;

As per claims 46 and 47, the further limitations of writing
a system administrator password that allows hidden memory area
contents or a recovery password to be reset is equivalently
taught by Junya as an error check circuit of the data storage 100
detects an error in password address read out from the password
table area 15 of the memory 10, the password address is replaced
by prescribed data (e.g. FFFF) to indicate its unreliability
(e.g. see column 3, lines 34-39);

Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which
forms the basis for all obviousness rejections set forth in this
Office action:

> (a) A patent may not be obtained though the invention is
> not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the
> subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been
> obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject
> matter pertains. Patentability shall not be negatived by
> the manner in which the invention was made.

6.   Claims 31, 44 and 49-60 rejected under 35 U.S.C. 103(a) as

being unpatentable over Junya (USPN: 5,469,564);

As per claim 31, Junya disclose the invention as claimed,

detailed above with respect to claims 25-28, Junya however does

not particularly teach the hidden banks/blocks include a swap

space for copying data between the memory banks/blocks. First

of all, Junya discloses in one other embodiment of his invention

that rather than the passwords being stored in separate memory

blocks/banks of a flash EEPROM, all of the passwords could be

stored in the same memory block leaving other banks/blocks for

spare (e.g. see column 4, lines 24 et seq.). Therefore, it

would having been obvious to one having ordinary skill in the

art at the time the current invention was made to use the spare

blocks as a working storage space for copy the original

data/password in order to work on. In doing so, it would (a)

avoid the degradation of the original data, (b) minimize error

in which original data can not be modified which results to

enhancing of system reliability, therefore being advantageous;

As per claim 44, Junya discloses memory storage unit 10 is

dividing into a password area 15 and a data file area 16 for

storing active (valid reference) passwords (e.g. see Junya's

figure 1, column 2, lines 23-24; also see lines 34 et seq.).

Junya however does not particularly teach a swap space for

copying data between the memory banks/blocks. First of all,

Junya discloses in one other embodiment of his invention that

rather than the passwords being stored in separate memory

blocks/banks of a flash EEPROM, all of the passwords could be

stored in the same memory block leaving other banks/blocks for

spare (e.g. see column 4, lines 24 et seq.). Therefore, it

would having been obvious to one having ordinary skill in the

art at the time the current invention was made to use the spare

blocks as a working storage space for copy the original

data/password in order to work on. In doing so, it would (a)

avoid the degradation of the original data, (b) minimize error

in which original data can not be modified which results to

enhancing of system reliability, therefore being advantageous.

As per claims 49-56; they encompass the same scope of

invention as to that of claims 40-48; however, Junya do not

particularly disclose a computer-readable medium of instructions

to be implemented on a computer as being claimed 49-56.

However, one of ordinary skill in the art would have recognized

that computer readable medium (i.e., floppy, cd-rom, etc.)

carrying computer-executable instructions for implementing a

method is generally well-known in the art, because it would

facilitate the transporting and installing of the method on
other systems. For example, a copy of the Microsoft Windows
operating system can be found on a CD-ROM from which Windows can
be installed onto other systems, which is a lot easier that
running a long cable or hand typing the software onto another
system. The examiner takes Official Notice of this teaching.
Therefore, it would have been obvious to put Junya's program on
a computer readable medium, because it would facilitate the
transporting, installing and implementing of Junya's program on
other systems.

     As per claim 57, <u>Junya</u> teaches the invention as claimed
including a system comprising a memory device 100 comprising a
main memory array is taught as flash memory array 10 (e.g. see
figure 1; column 2, lines 21 et seq.); an internal processor to
execute programming code is taught as the R/W control circuit 11
for executing programming code from host computer 200 (e.g. see
figure 1); a hidden storage area connected to the main flash
array wherein the programming code prevents access to the hidden
storage area without a valid password is taught by Junya as the
read/write control circuit 11 functions to read passwords from
the data file area 16 of the memory 10 in response to address
signals generated by the address signal generator 13 based upon
the password addresses read from the password table area 15; the
comparing circuit 12 functions to compare the passwords read out

by the read/write control circuit 11 with the password supplied
by the host computer 200; wherein if the comparing circuit 12
detects a match, the data storage device 100 provides an access
permission signal to the host computer 200 for access to memory
10. (e.g. see abstract, column 2, lines 34 et seq.; lines 65
bridging column 3, line 4). Junya, however does not particularly
discloses a wireless communication transceiver known to allow the
system to operate in a wireless environment. First of all, it
should be noted that Junya, starting at column 4, lines 35 et
seq, clearly discloses that many variations and/or modifications
could have been implemented to the invention without changing its
scope which known to including the making of Junya's system to
operate in the wireless environment as being claimed as
Applicant. Accordingly, it would have been obvious to one having
ordinary skill in the art at the time the current invention was
made to make the system of Junya to operate in the wireless
environment by adding the wireless transceiver. In doing so, it
would increase the flexibility of Junya's system by allowing it
to serve a broader range of applications and their (variants)
thereby broadening one's potential market and saving investment
capital.

As per claims 58 and 59, Junya discloses main memory array
is a flash EEPROM; noting that Junya further discloses the type
of memory employed is NOT limiting to the present invention (e.g.
see column 2, lines 24-26);

As per claim 60; the further limitation of where the hidden
storage area of memory array 100 comprises one or more hidden
banks is taught by Junya to the extent that it is being claimed,
for example, as noted above, the type of memory is a system
depended feature, wherein as being illustrated by Junya; any
type of memory could be implemented including DRAM, RAM, FLASH,
which is known to comprise at least one segment/bank/portion as
being claimed (e.g. see column 2, lines 24-26);

7.   With respect to the remark, the concept of internal
processor for executing the programming code is taught by Junya
to the extent that it is being claimed; for example, the control
circuit 11 as cited to be equivalent to the internal processor
for processing and read the active password addresses (which are
preferably encoded) from the password table area 15 of the
memory 10 when the host computer 200 issues a read or write
request (i.e., a data access request) and supplied to the
address signal generator 13, which functions to decode the
active password addresses (if they are encoded) and to generate
the absolute or actual active password addresses (e.g. see
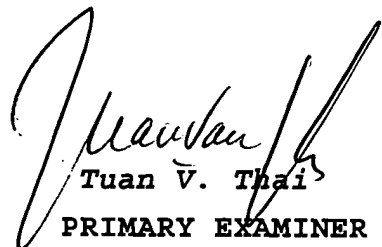column 3, lines 21 et seq.).

Conclusion

8.   The prior art made of record and not relied upon is
considered pertinent to applicant's disclosure.

9.   Any inquiry concerning this communication or earlier
communications from the examiner should be directed to Tuan V.
Thai whose telephone number is (571)-272-41287. The examiner can
normally be reached from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are
unsuccessful, the examiner's supervisor, Mathew M. Kim can be
reached on (571)-272-4182. The fax phone number for the
organization where this application or proceeding is assigned is
703-872-9306. Information regarding the status of an application
may be obtained from the Patent Application Information Retrieval
(PAIR) system. Status information for published applications may
be obtained from either Private PAIR or Public PAIR. Status
information for unpublished applications is available through
Private PAIR only. For more information about the PAIR system,
see http://pair-direct.uspto.gov. Should you have questions on
access to the Private PAIR system, contact the Electronic
Business Center (EBC) at 866-217-9197 (toll-free).

TVT/December 07, 2004

Tuan V. Thai
PRIMARY EXAMINER
Group 2100